REMARKS

The outstanding Office Action of Oct. 18, 2005 objected claim 10 for an informality and rejected claims 1-13 as allegedly being anticipated by *Toda* (USP 5,010,518) or being obvious over *Toda* in view of Applicant Admitted Prior Art (AAPA) and *Loo* (USP 5,845,325). For at least the reasons set forth herein, Applicant disagrees and requests reconsideration and withdrawal of the rejections.

Cosmetic Amendments to Claims 10 and 11

"Active" in claim 10 is replaced with "activate" as suggested by the Examiner. Furthermore, a redundant term "and" in claim 11 is removed. It is believed the amendments add no new matter and the claim objection is overcome.

Response To Claim Rejections Under 35 U.S.C. §102

Claims 1-2 and 4 stand rejected under 35 U.S.C. §102(b) as allegedly anticipated by *Toda*. Applicant respectfully traverses this rejection on the grounds that *Toda* does not disclose, teach, or suggest all of the claimed elements.

For a proper rejection of a claim under 35 U.S.C. Section 102(b), the cited reference must disclose all elements/features/steps of the claim. *See, e.g., E.I. du Pont de Nemours & Co. v. Phillips Petroleum Co.*, 849 F.2d 1430, 7 USPQ2d 1129 (Fed. Cir. 1988). For anticipation, there must be no difference between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention. *See, e.g., Scripps Clinic & Res. Found. v. Genentech, Inc.*, 927 F.2d 1565, 18 USPQ 2d 1001 (Fed. Cir. 1991.)

Independent 1, as originally filed, states:

1. A memory unit, comprising:

first and second access transistors coupled to a bit line pair, wherein ***the first access transistor comprises a first terminal coupled to one bit line pair,*** and ***the second access transistor comprises a first terminal coupled to the other;***

a latch node coupled between second terminals of the first access transistor and the second access transistor to latch data; and

a selection unit having two input terminals coupled to a word line and a flush line, and an output terminal coupled to gates of the first access transistor and the second assess transistor, wherein predetermined information is written to the latch node from the bit line pair according to activations of the word line or the flush line.

(*Emphasis added*).

Applicant submits that independent claim 1 is allowable for at least the reason that *Toda* does not disclose, teach, or suggest the features that are emphasized in claim 1 above. More specifically, as emphasized above, each of the first and second transistors in claim 1 has two different terminals, including a first terminal coupled to one bit line pair and a second terminal coupled to a latch node. The access transistors in *Toda*, referred by the Office Action, are transistors DS1 and DS2 in Fig. 1D, and each, however, has only one common terminal coupled to both one bit line pair and a latch node. Referring to Fig. 1D of *Toda*, the transistor DS1 has one terminal ND coupled to bitline BL1-bar. Even though the Office Action did not explicitly indicate where a latch node is in *Toda*, the sense amplifier SA1 with two inverters seems to be referenced. The transistor DS1 uses the same terminal ND to couple to amplifier SA1, as shown in Fig. 1D of *Toda*. In other words, there are no two terminals of the transistor DS1 respectively coupled a latch node and one bit line pair as required in claim 1 of the present application. As *Toda* does not disclose, teach or suggest all elements in the claim 1 of the present application, *Toda* fails to anticipate the claim 1, and for at least this reason the rejection should be withdrawn.

In addition, *Toda* fails to disclose the selection unit featured in claim 1, which must have one input terminal coupled to a word line. The Office Action referred to OR gate 120 in Fig. 1D of *Toda* as being the selection unit of claim 1. The input terminals of OR gate 120 are DCST and a signal line from the flush write mode timing generator 122, and none of them is coupled to a word line, such as wordlines WL1, WL2, WL1-bar, WL2-bar in Fig. 1D of *Toda*. Clearly, OR gate 120 of *Toda*, which has no input terminal coupled to a wordline, cannot read on the selection unit of claim 1, which need an input terminal coupled to a wordline. Since *Toda* does not disclose, teach or suggest all elements in the claim 1 of the present application, *Toda* fails to anticipate the claim 1, and the rejection should be withdrawn.

Further, *Toda* is non-analogous to the present application. What *Toda* discloses is a technology concerned with "a cell data sense circuit for a non-volatile semiconductor memory using a ferroelectric cell and requiring no refresh operation." *See* the section of "the Field of the Invention" of *Toda*. The present application, in the other hand, is concerned with "a cache memory", which, as taught in the specification, usually uses SRAM cells, a kind of a volatile semiconductor memory. Toda's technology for non-volatile semiconductor memories is non-analogous to a technology for volatile semiconductor memories.

Toda fails to recognize the advantages of Applicant's claimed invention. The memory units in the embodiment of the present application have real synchronous elements and are "less sensitive to signal glitch, system noise, manufacture process and so on." Lines 14-15, page 7. Furthermore, embodiments of the present application are "well suitable to timing analysis, since the state of the latch nodes is changed by controlling the gate side of the access transistor without drain/source side." Lines 16-18, page 7. The memory module of the present application is "applicable to direct-mapping storage, set-associative mapping storage and full-associative

mapping storage." Lines 20-21, page 7. Since *Toda* discloses a non-analogous art regarding to a non-volatile semiconductor memory, *Toda* does not discuss problems about a cache memory, not to mention the advantages achieved by Applicant's invention.

Thus, *Toda* does not anticipate claim 1, and the 102(b) rejection should be withdrawn.

As independent claim 1 is allowable over the prior art of record, then its dependent claims 2 and 4 are allowable as a matter of law, because these dependent claims contain all features/elements/steps of their respective independent claim 1. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

Response To the 103 rejections of Claims 3, 5-9 and 11-13

Claims 3, 5-9 and 11-13 stand rejected under 35 U.S.C. §103(a) as allegedly unpatentable over *Toda* in view of AAPA. Applicant respectfully traverses this rejection on the grounds that *Toda* and AAPA cannot establish a prima facie case of obviousness.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Each of the rejections of claim 3, 5-9 does not meet all the three criteria such that a prima facie case of obviousness is not established and the rejections should be withdrawn.

First, there is no proper motivation or suggestion in *Toda* or AAPA for combination or modification. As mentioned before, *Toda* is non-analogous to the present application and there is no reason for a person of a skill in the art to reference *Toda*, regarding to non-volatile memory technology, for modifying the teaching of AAPA, regarding to volatile memory technology. Neither does *Toda* figure out or solve the problems mentioned in AAPA. Thus, *Toda* and AAPA cannot be references for a prima facie case of obviousness.

Second, there is no reasonable expectation of success. Even if a person skilled in the art references *Toda* and AAPA, he/she has no idea how to combine or modify the teachings in *Toda* and AAPA and create the claimed invention in the present application. *Toda* and AAPA are so different and unrelated such that a person skilled in the art cannot expect where to start for modification. There is no sign in *Toda* and AAPA showing that any possible combination or modification from *Toda* and AAPA will work.

Third, *Toda* and AAPA, even if combined, do not teach or suggest all the claim limitations.

a) Claim 3

Claim 3 depends from independent claim 1. Similar with the previous discussion for the patentability of claim 1, neither *Toda* nor AAPA discloses, teaches, or suggests the selection unit featured in claim 1 and claim 1 should be allowable in view of *Toda*, AAPA or the combination thereof. Since claim 3 contains all features/elements/steps of independent claim 1, *Toda* and AAPA still fail to disclose, teach or suggest all the claim limitations in claim 3, not meeting the third criteria for establishing a prima facie case of obviousness. Therefore, the 103 rejection for claim 3 should be withdrawn.

b) Claims 5-9

Independent 5, as originally filed, states:

> 5. A memory module, comprising:
> at least one first memory region comprising a plurality of memory units, each memory unit comprising:
> first and second access transistors coupled to a bit line pair, wherein the first access transistor includes a first terminal coupled to one of the bit line pair, and the second access transistor includes a first terminal coupled to the other;
> a latch node coupled between second terminals of the first access transistor and the second access transistor to latch data; and
> ***a selection unit including a first input terminal coupled to a word line,*** an output terminal coupled to gates of the first access transistor and the second assess transistor, and a second input terminal;
> wherein the second input terminals of the selection units in all memory units are coupled to a flush line, and invalidation information is written into the latch nodes in the memory units from the bit line pair when the flush line is activated during a flush operation.

(*Emphasis added*).

Independent claim 5 defines the same selection unit, as defined claim 1. Therefore, similar to the previous discussion for the patentability of claim 1, neither *Toda* nor AAPA discloses, teaches, or suggests the selection unit as highlighted above in claim 5 and claim 5 should be allowable in view of *Toda*, AAPA or the combination thereof.

As independent claim 5 is allowable over the prior art of record, then its dependent claims 6-9 are allowable as a matter of law, because these dependent claims contain all features/elements/steps of their respective independent claim 5. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

c) Claims 11-13

Independent 11, as slightly amended for informality, states:

> 11. A fabricating procedure for a cache memory, comprising:

determining conditions for a tag memory in the cache memory according to a desired specification of the cache memory;

implementing the tag memory as a memory module according to determined conditions, wherein tag memory comprises a plurality of memory units, each comprising:

first and second access transistors coupled to a bit line pair, wherein the first access transistor comprises a first terminal coupled to one bit line pair, and the second access transistor comprises a first terminal coupled to the other;

a latch node coupled between second terminals of the first access transistor and the second access transistor to latch data; and

an OR gate comprising two input terminals coupled to a word line and a flush line, and an output terminal coupled to gates of the first access transistor and the second assess transistor, wherein invalidation information is written to the all latch nodes in the memory units from the bit line pair according to activation of the flush line;

checking whether the implemented tag memory meets the determined conditions;

implementing peripheral elements in the cache memory according to the desired specification of the cache memory;

modifying the peripheral elements to match the tag memory such that the peripheral elements meet the desired specification; and

simulating integration of the tag memory and the peripheral elements in the cache memory to ensure compliance thereof with the desired specification.

(*Emphasis added*)

Independent claim 11 is allowable for at least the reason that *Toda*, AAPA or the combination thereof does not disclose, teach, or suggest the features that are highlighted in claim 11 above. More specifically, the OR gate emphasized above in claim 11 is an embodiment of a selection unit as defined in claim 1, which is never disclosed, taught, or suggest by *Toda* or AAPA (as discussed in connection with claim 1).

Furthermore, neither *Toda* nor AAPA discloses and teaches all the steps in claim 11; such as determining, implementing, checking, modifying and simulating. Please note that what claimed in claim 11 is a fabricating procedure. *Toda* and AAPA might teach structures of memories, but none of them discloses or teaches what kind of steps is needed to take for implementing the structures. Therefore, notwithstanding the lack of required motivation and expected success in

Toda and AAPA, claim 11 should be allowable since *Toda* and AAPA do not teach all the steps in claim 11.

As independent claim 11 is allowable over the prior art of record, then its dependent claims 12-13 are allowable as a matter of law, because these dependent claims contain all features/elements/steps of their respective independent claim 11. *In re Fine*, 837 F.2d 1071 (Fed. Cir. 1988).

Response To the 103 rejection of Claims 10

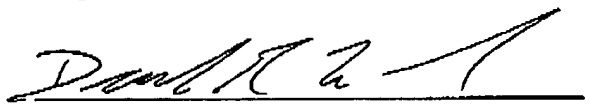
Claims 10 stands rejected under 35 U.S.C. §103(a) as allegedly unpatentable over *Toda* in view of AAPA and *Loo*. Applicant respectfully traverses this rejection on the grounds that claim 10 depends to the independent claim 5, which is allowable as discussed above.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 1-13 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested.

If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned agent at (770) 933-9500.

Respectfully submitted,



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